

System Specification and Verification

- Seminar - Week 4 -

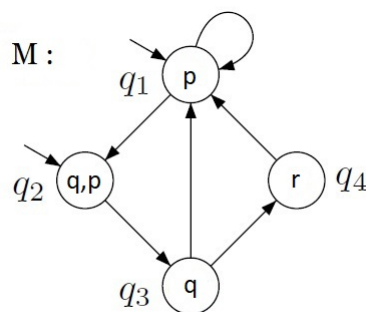
Spring 2026

- Let consider a boolean circuit with input x , output y and two registers r_1 and r_2 .

Translate the following properties as LTL formulas over $\mathcal{AP} = \{x, y, r_1, r_2\}$:

- "it is impossible to get two consecutive 1 as output"
- "each time the input is 1, at most two ticks later, the output will be 1"
- "each time the input is 1, the register contents remain the same over the next tick."
- "register r_1 is infinitely often 1"
- "register r_1 has a finite number of times value 1"
- "register r_1 has value 1 exactly one time".

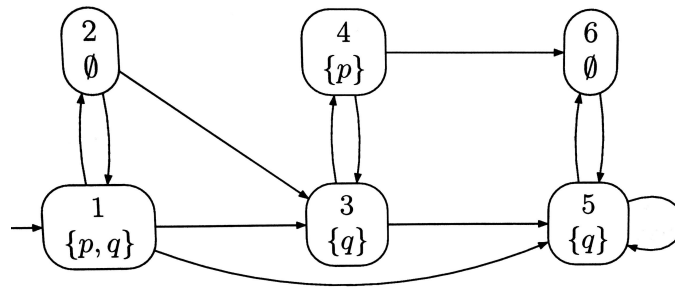
- Compute $\llbracket AXq \rrbracket$, $\llbracket EXp \rrbracket$ and $\llbracket E(qUr) \rrbracket$ in the following model:



- (CTL*) Are the following formulas equivalent?

- $AXAG\varphi$ and $AXG\varphi$
- $EXEG\varphi$ and $EXG\varphi$
- $A(\varphi \wedge \psi)$ and $A\varphi \wedge A\psi$

- (d) $E(\varphi \wedge \psi)$ and $E\varphi \wedge E\psi$
 (e) $\neg A(\varphi \rightarrow \psi)$ and $E(\varphi \wedge \neg\psi)$
4. (CTL equivalences) Verify if the formulas $\varphi_1 = AG(EFp)$ and $\varphi_2 = EFp$ are equivalent. If not, does one imply the other?
5. For the Labelled Transition System below, compute the following sets of states:



- (a) $\llbracket EFp \rrbracket$
 (b) $\llbracket AFq \rrbracket$
 (c) $\llbracket \varphi \rrbracket$ where $\varphi = E(q \mathcal{U} (p \wedge \neg q))$
 (d) $\llbracket \varphi \rrbracket$ where $EGq \vee (EGp \wedge EFq)$